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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,906	07/25/2001	Byoung Kwon Cha	000939-085400US	7303

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
NGUYEN, TAN	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,906	CHA, BYOUNG KWON	
	Examiner	Art Unit	
	Tan T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5 and 20-44* is/are allowed.

6)☒ Claim(s) *6-16,18,19 and 45-49* is/are rejected.

7)☐ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following action is in response to the Preliminary amendment filed by Applicant on July 25, 2001.

2. New claims 5-49 have been added.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification did not provide proper antecedent basis for claimed subject matter such as "a primary circuit" in claim 6, claim 16.

The specification also did not provide proper antecedent basis for the erase operation in claim 15.

The specification also did not provide proper antecedent basis for the programming parallel as in claims 18-19, and to write one bit at a time as in claim 46.

4. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 12, it is not clear how the Applicant determined M is two or less since the number of memory cell(s) that is not properly written is not predictable.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 6-10, 14, 16, 45-46, 47, 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohuchi et al. (U.S. Patent No. 5,657,270).

Regarding claims 6, 16, 45, 47, 49, Ohuchi et al. disclosed in Fig. 1 non-volatile memory device EEPROM [10] comprises a main memory array [12] (column 4, line 62), a data latch circuit [16] (column 4, line 67), a data comparator [22] (column 5, line 17), wherein the output of the data latch circuit [16] is connected to the first input of the data comparator circuit [22] (column 5, lines 16-17). The output of sense amplifier [18] is coupled to the second input of the data comparator circuit [22]. The output of the data comparator circuit [22] is fed back to the data latch circuit [16] via an output buffer circuit [24] (column 5, lines 16-21). Ohuchi disclosed that the data latch circuit [16] is provided for execution of data write in the EEPROM [10] (column 5, lines 1-3). Furthermore, Ohuchi et al. disclosed a data of "one word" is latched in the data latch circuit [16] at the start of the data write operation (column 10, lines 16-18). The "one word" latched in data latch circuit [16] would be N bits data. Therefore, the data latch circuit would be understood as the claimed input component.

Ohuchi et al. disclosed the data comparator circuit [22] compares a write data being latched by the data latch circuit [16] with a data read out by the sense amplifier circuit [18] in the verify operation performed during programming (column 5, lines 27-30; column 8, lines 10-13; column 11, lines 18-20). The verifying operation is executed with respect to each of the data written memory cell transistors arrayed along a designated word line [WLi] (column 10, lines 54-56). In column 11, lines 11-67, Ohuchi disclosed the verifying operation, wherein "1" data is latched again with respect only to specific

address or addresses at which data programming is still insufficient. With such "relatching" the data "1" writing is repeatedly executed, which may be called the "data "rewriting". Although Ohuchi et al. did not discuss the number of bits of data being rewritten, it is inherent that the number of rewriting bits of data is less than the number of bits of "one word" latched in the latch data circuit [16] because it is not possible for every bit in the selected word line being programmed insufficiently. Accordingly, the data comparator circuit [22] would be understood as the claimed primary circuit.

Regarding claims 7-8, Ohuchi disclosed the data comparator circuit [22] compares the write data being latched by the data latch circuit [16] with the data read out by the sense amplifier circuit [18](column 5, lines 28-30) to determine whether the write data has been sufficiently written to the selected memory cells.

Regarding claims 9-10, Ohuchi disclosed that the data rewriting being performed only to the memory cells which is insufficiently written (column 11, lines 57-62, claim 1, column 18, lines 25-27).

Regarding claim 14, Ohuchi et al. disclosed the "one word" that latched in the data latch circuit [16] is used for data write or programming (column 10, lines 16-18).

Regarding claim 46, Ohuchi et al. disclosed in NAND type EEPROM, data is sequentially written into the floating gate type MOSFETs (column 1, lines 60-61).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 11-13, 15, 18-19, 48, rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi et al..

See description of Ohuchi et al. in paragraph 4, supra. Ohuchi did not discuss the "one word" for data write is 2, 4, 8, 16, or 32.

Regarding claims 11, 13, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the data write operation of Ohuchi et al. by selecting an appropriate number of data bits of the "one word" for the data write (programming) operation.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to select an appropriate number of bits of data for the "one word" in the data write operation to optimize the write speed of the data write operation.

Regarding claim 12, as best understood, Ohuchi et al. showed in TABLE 1, the number of memory cells that are insufficiently written is two (the second and third bits).

Regarding claim 15, although the "one word" latched in the data latch circuit [16] is used for data write operation, it is known in the art that in erase operation, all of the cells would be first programmed to the same data of "1" or "0" before the actual erase operation.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the write operation of Ohuchi by using the data latched in the data latch circuit to perform erase operation.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to program all the memory cells to the same data "1" or "0" so that the threshold voltage of all the cells are uniform which reduces the over-erase cells.

Regarding claims 18-19, Ohuchi et al. did not discuss the data is written in parallel.. It is known in the art that one bit at a time or parallel writing have been used.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the data write operation of Ohuchi et al. by providing either the one bit at a time of parallel writing.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use parallel writing to reduce the writing time, or use the one bit at a time to reduce the writing error.

Regarding claim 48, it is known in the art that in verifying operation, bit-by-bit comparison would be used.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the verifying operation of Ohuchi by using the bit-by-bit comparison.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use the bit-by-bit comparison to thoroughly check every selected memory cell for error.

9. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 20-40, 41-44 are allowed.

The following is an examiner's statement of reasons for allowance:

Ohuchi et al. failed to show or suggest the combination of a comparator having a logic gate to output a first signal to indicate whether or not a reprogramming operation is need, and a controller coupled to the comparator and configured to output a second signal to initiate reprogramming of M number of the memory cells.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2818
December 23, 2004